Exam.Code:0921
Sub. Code: 6836

2021

B.E. (Information Technology)

Third Semester

ITE-375/344/304: Computer Architecture and Organization

Time allowed: 3 Hours

Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Explain the following:-

a) Name the type of instruction in IR register with binary value =1111001000000000.

b) Which instruction is considered as the hardware implementation of interrupt cycle?

c) Explain the term used to measure performance of cache memory.

d) Under which scenario polling procedure is used?

e) What are the three possible ways to specify AD field in symbolic microinstruction? (5x2)

UNIT – I

II. An instruction is stored at location 600 with its address field at location 601. The address field has the value 800. A processor register Rl contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct (b) immediate (c) relative (d) register indirect (e) index with Rl as index register also. (10)

III. a) Write symbolic microprogram for AND instruction.

b) With the help of diagram explain how selection of address for control memory is done? (4,6)

IV. Explain the various phases of instruction cycle with the help of flowchart. (10)

UNIT – II

V. Explain with the help of diagram how address mapping in virtual memory is performed using paged system. (10)

P.T.O.

VI. Why the read and write control lines in a DMA controller are bidirectional? Explain the working of DMA controller with the help of block diagram. (10)

VII. a) In a multistage switching network with 2*2 switches build a binary tree to connect a processor PI with destination Oil.

b) What are the various advantages and disadvantages of multiport memory and crossbar switch? (5,5)

x-x-x