Exam.Code:0975
Sub. Code: 7424

2031

M. Tech. (Micro-Electronics)

First Semester

MIC-104: HDL and VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) What is VLSI design digital system?

b) Explain the trends in HDLs?

c) Differentiate between signal assignment and variable assignment statements.

d) What are the primitive gates supported by Verilog HDL?

e) What is Rise, Fall and turn-off delays? (5x2)

UNIT - I

II. With syntax explain conditional, branching and loop statements available in Verilog HDL behavioural description. (10)

III. Apply the top-down design methodology to demonstrate the design of ripple carry counter. (10)

IV. List and explain the advantages and shortcomings of using VHDL? (10)

UNIT - II

V. What are the Subprograms in VHDL? Explain them in brief with suitable example. (10)

VI. Write Verilog HDL program to simulate traffic signal controller. Also write the stimulus for the same. (10)

VII. Define the term' State Machine'. Write Verilog HDL program of 4-bit asynchronous up counter. (10)

x-x-x