Exam.Code:0970
Sub. Code: 7347

1059

M.E. (Electronics and Communication Engineering)
Second Semester
ECE-1205: VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) Briefly discuss LOCOS process.

b) Draw VLSI design flow diagram.

c) List various functions performed in Data Path subsystems.

d) Briefly discuss Ratioed circuits.

e) How HDLs are useful in IC design? (5x2)

UNIT – I

II. Explain the structure and operation of MOSFET. Derive the I-V relationship for MOS transistor. Also discuss ideal and non-ideal I-V characteristics of MOSFET. (10)

III. a) Explain Min-Delay and Max-Delay constraints with appropriate examples.

b) Explain concept of Pass Transistor Logic and list applications of it. Also discuss charge sharing problem. (5,5)

IV. a) Explain CMOS implementation of D-Latch along with its timing diagrams.

b) List various types of data path subsystems. Explain working of Barrel Shifter. (5,5)

UNIT – II

V. Explain three design domains of VLSI design in detail using neat diagram of Y chart. (10)

VI. a) Discuss global and switchbox routing in detail.
b) Discuss timing driven placement along with flow diagram. (2x5)

VII. Write Short note on following:-

a) Layout Synthesis
b) SPICE simulation
c) Floorplanning
d) Clock distribution (4x2½)

x-x-x