Exam. Code: 0921

Sub. Code: 6836

1079

B. Engg. (Information Technology) 3rd Semester

ITE-375/304: Computer Architecture & Organization

: 3 Ho	urs Max. Marks: 50
Attem seleci	apt <u>five</u> questions in all, including Q. No. 1 which is compulsory and ting atleast two questions from each Unit. -*-*-*-
Atten	npt the following: -
(a)	What are the consideration for a system design?
(b)	Define the term Hit Ratio.
(c)	Define the term microinstruction.
(d)	Differentiate between synchronous & asynchronous data transfer.
(e)	Define the term locality of reference. (5×2)
	<u>UNIT-I</u>
(a)	What do you understand by Gate Level and Register Level Design? Discuss in brief.
(b)	The content of PC in the basic computer is 3AF. The content of AC is 7EC3. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.
	(i) What is the instruction that will be fetched and executed next?
	(ii) Show the effect of instruction of AC if the operation to be
	performed i AND. (5+5)
(a)	Explain the different phases of instruction cycle.
(b)	Discuss the design of Accumulator logic and draw the circuit associated
	with it. (5+5)
(a)	What do you mean by micro-programmed control unit? Explain with example.
(b)	Explain the major characteristics of RISC & CISC. (5+5)
	Attent selection (a) (b) (c) (d) (e) (a) (b)

UNIT-II

- V. Discuss the different mapping techniques used in cache memory & their relative merits & demerits.
- VI. (a) What is the need for DMA controller? Draw and explain its block diagram.
 - (b) Draw a flow chart that describes CPU-I/O channel communication. (5+5)
- VII. (a) What do you mean by parallel processing? What are the characteristics of multiprocessors? Discuss.
 - (b) Differentiate between isolated I/O and memory mapped I/O.

 [5+5]