Exam. Code: 0969
Sub. Code: 7339

1079

M.E. Electronics & Communication Engineering-1st Semester

ECE-1104: Digital System Design

Time allowed: 3 Hours | Max. Marks: 50

NOTE: *Attempt* ***five*** *questions in all, including Q. No. 1 which is compulsory and selecting atleast* ***two*** *questions each from Part-A & B.*

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1. Attempt the following: 5 X 2 =10
   a. Give two points of difference between CPLDs and FPGAs.
   b. What is critical race in asynchronous sequential circuits?
   c. What is the difference between a Moore machine and a Mealy machine?
   d. What is the BIST technique?
   e. What are stuck- at faults?

PART-A

2. a) Implement the logic function F(A, B, C, D) =∑(0, 1, 3, 4, 8, 9, 15) using a 8 x 1 multiplexer.
   b) Describe the various specifications of a D/A converter. 2 X 5 =10

3. a) What is a decoder? What are its applications? Explain the design of BCD-to-seven segment decoders.
   b) Implement the following logic expression using an elementary ROM and PLA.
   F = ∑(0,1,3,4,7) 2 X 5 =10

4. a) Write a VHDL program for a 1-bit comparator using dataflow modelling.
   b) What are the various blocks of an ALU? How can it be implemented on an FPGA? Explain briefly. 2 X 5 = 10

PART – B

5. a. Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected.
   b. What are the phases of design while designing system controller? How is the controller architecture chosen? 2 x 5 = 10

6. Design a synchronous finite state machine which will sequence from state *a* =00 to state *b*=11 to state *c*=10 to state *d*=01, then reverse itself at state *a* and state *d* if the input COSQ(H) is asserted. Any time the COSQ input is not asserted, the circuit is to revert to state *a* and hold. Carry out all necessary steps for the design. Make your choice of flip-flops based on minimal cost next state decoder implementation. 1 X 10 =10

7. Write short notes on: 2 X 5 = 10
   a) Internal scan test methodology
   b) JTAG scan techniques

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