Exam.Code:0932
Sub. Code: 6938

1019

B.E. (Electronics and Communication Engineering)

Eighth Semester

EC-802: HDL Based Systems

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Attempt the following:-

a) Logic Design

b) Hazards

c) Array

d) Entity

e) Tristate logic

f) Adder

g) Mapping

h) Place and Route

i) Synthesis

j) Multiplier (10x1)

UNIT – I

II. Explain Modelling of flip flops using VHDL processes and VHDL delays. (10)

III. Define state reduction. What are the rules for state reduction? Explain Instate logic and busses with the help of diagrams. (10)

IV. Explain Finite state Machines and also explain its categories with the help of example. (10)

UNIT – II

V. a) A combinational circuit is defined by the functions:-

i) $F_1 (A,B,C)=\Sigma(3,5,6,7)$

ii) $F_2 (A,B,C)=\Sigma(0,2,4,7)$

Implement circuits with a PLA having three inputs, four product terms, and two outputs.

b) Explain the salient features of FPGAs.

c) Explain the difference between CPLD and FPGA. (4,3,3)

P.T.O.

VI. Design Traffic light controller. (10)

VII. Explain the following in context with FPGA:

a) Carry chains
b) Cascade chains (10)
c) Multiplier

x-x-x