1129

M. Tech. (Micro-Electronics) First Semester

MIC-103: MOS Integrated Circuit Modeling

Time	allowed:	3	H	ou	rs
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Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed. X-X-X

(Q1.	Answ	er the following:-	2)	
		(a)	What will be amount of current flowing between source and drain region of MOSFET (2)	
		, ,	I an Appletion aurien width on draw and course side is could!	(2)	
		(b)	Design 2-bit multiplexer using MOS transistors.	(2)	
		(c)	The CMOC NAME agts of CMOS NOR Raige	(2)	
		-	What is the effect on depletion charge density, oxide potential if body of n-channel ((4)	
		(d)	MOS capacitor is connected to a positive power supply?	(2)	
			MOS capacitor is connected to a positive power supply? Why MOSFET is not used in accumulation region, even charge carriers are present in	(2)	
		(e)	Why MOSPET is not used in decommend		
			channel?		
			SECTION A		
				(5)	
			Design the Full adder circuit using CMOS transmission gate. Design the Full adder circuit using CMOS transmission gate.	(5)	
Q2.		(a)	Design the Full adder circuit using CMOS transmission gate. Derive equation for the gain of Resistive Load Inverter and discuss effect of	(-,	
		(b)	Derive equation for the game	(5)	
			transconductance. Derive MOSFET current equation in different regions of operations. Derive MOSFET is not preferred beyond 32 nm technology? Discuss	(5)	
Q3.		(a)	Derive MOSFET current equation in different regions of operations. Why conventional MOSFET is not preferred beyond 32 nm technology? Discuss		
		(b)	Why conventional World to the world with the world	(5)	
			limitations in detail. Design a resistive-load inverter with $R = 1 \text{ k}\Omega$, such that $V_{OL} = 0.6 \text{ V}$. Design a resistive-load inverter with $R = 1 \text{ k}\Omega$, such that $V_{OL} = 0.6 \text{ V}$.		
	Q4.	(a)	Design a resistive-toad inverter transistor has the parameters:		
	~		Design a resistive-load inverter with $R = 1 \text{ KY}$, such that \sqrt{c} . Design a resistive-load inverter with $R = 1 \text{ KY}$, such that \sqrt{c} . The enhancement-type nMOS driver transistor has the parameters: The enhancement-type nMOS $V_{\text{res}} = 0.2 \text{ V}^{1/2}$, $\lambda = 0$, $\mu_{\text{n}} C_{\text{ox}} = 22.0 \mu \text{A/V}^2$.		
			$V_{DD} = 5.0 \text{ V}, V_{T0} = 1.0 \text{ V}$		
			(a) Determine the required by those	(5)	
			(a) Determine V _{IL} and V _{IH} . (b) Determine V _{IL} and V _{IH} . (c) Determine V _{IL} and V _{IH} . (d) Determine V _{IL} and V _{IH} . (e) Determine V _{IL} and V _{IH} . (f) Determine V _{IL} and V _{IH} . (g) Determine V _{IL} and V _{IH} .		
		(b)	Discuss the problems by depletion load MOS Inverter: Draw today		
			(b) Determine V _{IL} and V _{III} . (b) Determine V _{IL} and V _{III} . Discuss the problems associated with linear load MOS inverter and not inverted by depletion load MOS Inverter? Draw load characteristic of problems are resolved by depletion load MOS Inverter.		
			depletion load William		
			SECTION B		
			- CMOS inverter.	(5)	
			Derive equation for the low noise margin of a CMOS inverter. Derive equation for the low noise margin of a CMOS inverter. Derive equation for the low noise margin of a CMOS inverter.	(5)	
	Q5	. (a	Derive equation for the low noise margin of a CNIOS transistors. Discuss applications and limitations of BiCMOS transistors. Discuss applications and limitations of BiCMOS transistors. A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 10^{20} \text{ cm}^{-3}$, $Q_0/q = 4 \times 10^{10} \text{ cm}^{-3}$.	(5)	1
		(t	Discuss appreciated was fabricated on an n-type substitute $\frac{10^{20} \text{ cm}^3}{\text{cm}^3}$, $\frac{Q}{Q} = 4 \times 10^{10} \text{ cm}^3$		
	Q	j. (i	Discuss applications and limitations of Discuss applications and limitations and limitations of Discuss applications and Discuss and Discuss and Discuss applications and Discuss and Discuss and Discuss and Discuss and Discuss and Discuss an	m	
`			$N_D = 10^{\circ}$ cm ² , gate t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 0.1 μ m. Calculate the difference and gate oxide thickness of t_{co} = 1.5 V and V_{DS} = 3 V . Use t_{co} = 11.7 t_{co} .	. , , c	,
			and gate $0.000 = 0.000 = 1.5 \text{V}$ and $0.000 = 0.000 = 0.000$ latch circuit. How the outp	ut (5)
			and gate oxide thickness of the and V _{DS} = 3V. Use $\varepsilon_{si} = 11.7 \varepsilon_{0}$. temperature for V _{SB} = 0, V _{GS} = 1.5V and V _{DS} = 3V. Use $\varepsilon_{si} = 11.7 \varepsilon_{0}$. temperature for V _{SB} = 0, V _{GS} = 1.5V and V _{DS} = 3V. Use $\varepsilon_{si} = 11.7 \varepsilon_{0}$. Discuss and draw the CMOS AOI realization of the JK latch circuit. How the outp		
		(b) Discuss and draw the like latch configuration?	nd (2	.)
			b) Discuss and draw the CMOS AOT realizable toggles in this JK latch configuration? toggles in this JK latch configuration? a) Rise time of CMOS inverter is higher than fall time if aspect ratios of the nMOS as toggles in this JK latch configuration? Bise time of CMOS inverter is higher than nMOS in CMOS inverted.	,-	21
C		7. (a) Rise time of Civios in the pMOS transistor are same, why? pMOS transistor are same, why? pMOS transistor are same, why?	er, (3) 1
`			pMOS transistor are such as pMOS is 2.5 times night than		6
		(a) Rise time of CMOS inverter is higher than nMOS in CMOS inverted pMOS transistor are same, why? b) Preferred channel width of pMOS is 2.5 times higher than nMOS in CMOS inverted with the preferred channel width of pMOS is 2.5 times higher than nMOS in CMOS inverted with the preferred channel width of pMOS is 2.5 times higher than nMOS in CMOS inverted with the pMOS transistor has parameters W=10μm, L=1μm, channel length modulate why? c) A nMOS transistor has parameters W=10μm, L=1μm, channel length modulate why? c) O 24V⁻¹, t_{xy}=8 nm, V_{To}=0.6 V, N_a=5x10¹⁵ cm⁻³. Calculate the dr 	ion (5)
			why? W=10μm, L=1μm, Calculate the dr	ain	
		((c) A nMOS transistor has plan, $V_{T_0} = 0.6 \text{ V}$, $N_s = 5 \times 10^{-2} \text{ cm}$		
		`	parameter is 0.0247 3		
			Scurrent for $V_{SB} = 0$.		