Exam.Code:0975
Sub. Code: 7423

1129

M. Tech. (Micro-Electronics)
First Semester
MIC-103: MOS Integrated Circuit Modeling

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Section. Use of scientific calculator is allowed.

X-X-X

Q1. Answer the following:-

(a) What will be amount of current flowing between source and drain region of MOSFET when depletion region width on drain and source side is equal? (2)

(b) Design 2-bit multiplexer using MOS transistors. (2)

(c) Which is better and why – CMOS NAND gate or CMOS NOR gate? (2)

(d) What is the effect on depletion charge density, oxide potential if body of n-channel MOS capacitor is connected to a positive power supply? (2)

(e) Why MOSFET is not used in accumulation region, even charge carriers are present in channel? (2)

SECTION A

Q2. (a) Design the Full adder circuit using CMOS transmission gate. (5)

(b) Derive equation for the gain of Resistive Load Inverter and discuss effect of transconductance. (5)

Q3. (a) Derive MOSFET current equation in different regions of operations. (5)

(b) Why conventional MOSFET is not preferred beyond 32 nm technology? Discuss limitations in detail. (5)

Q4. (a) Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement-type nMOS driver transistor has the parameters: V_{DD} = 5.0 V, V_{To} = 1.0 V, γ = 0.2 $V^{1/2}$, λ = 0, $\mu_n C_{ox}$ = 22.0 $\mu A/V^2$
(a) Determine the required aspect ratio, W/L.
(b) Determine V_{IL} and V_{IH}. (5)

(b) Discuss the problems associated with linear load MOS inverter and how those problems are resolved by depletion load MOS Inverter? Draw load characteristic of depletion load MOS Inverter.

SECTION B

Q5. (a) Derive equation for the low noise margin of a CMOS inverter. (5)

(b) Discuss applications and limitations of BiCMOS transistors. (5)

Q6. (a) A pMOS transistor was fabricated on an n-type substrate with a bulk doping density of $N_D = 10^{16}$ cm^{-3}, gate doping density (n-type poly) of $N_D = 10^{20}$ cm^{-3}, $Q_f/q = 4x10^{10}$ cm^{-1} and gate oxide thickness of t_{ox} = 0.1 μm. Calculate the threshold voltage at room temperature for V_{SB} = 0, V_{GS} = 1.5V and V_{DS} = 3V. Use $\varepsilon_{si} = 11.7\ \varepsilon_o$. (5)

(b) Discuss and draw the CMOS AOI realization of the JK latch circuit. How the output toggles in this JK latch configuration? (2)

Q7. (a) Rise time of CMOS inverter is higher than fall time if aspect ratios of the nMOS and pMOS transistor are same, why? (3)

(b) Preferred channel width of pMOS is 2.5 times higher than nMOS in CMOS inverter, why? (5)

(c) A nMOS transistor has parameters W=10μm, L=1μm, channel length modulation parameter is $0.024V^{-1}$, t_{ox}=8 nm, V_{To}=0.6 V, N_a=$5x10^{15}$ cm^{-3}. Calculate the drain current for V_{SB} = 0.

X-X-X