Exam.Code:0975
Sub. Code: 7424

1129

M. Tech. (Micro-Electronics)
First Semester
MIC-104: HDL and VLSI Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Attempt the following:-

a) What is meant by hardware Synthesis?

b) List various elements of VHDL.

c) Differentiate between sequential and concurrent assignments.

d) Differentiate predefined and user defined attributes.

e) How signal assignment is different from variable assignment? (5x2)

UNIT – I

II. a) Discuss various EDA tools used by VLSI industry? What are the expectations of EDA customers?

b) Discuss complete IC design flow. (2x5)

III. a) Discuss various data objects and data types in VHDL with syntax.

b) Design decade counter and write VHDL code using behavior modeling. (2x5)

IV. a) Discuss various design suites of VHDL using suitable example.

b) Discuss operators in VHDL and write code for 3-bit shift register using operators. (2x5)

UNIT – II

V. a) Explain FPGA based design flow steps.

b) Discuss important building blocks of FP'GA. (2x5)

VI. a) Discuss importance of FSM. What are the various types of FSM?

b) Design 3-bit asynchronous up-counter using FSM and write VHDL code. (2x5)

VII. Discuss various types of FSM. Write VHDL code for 101 sequence detector using behavioral Modeling (10)

x-x-x