Exam.Code:0999
Sub. Code: 7622

1129

M.E. (Computer Science and Engineering)
First Semester
Elective – II
CS-8109: Advanced Computer Architecture

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Unit.

x-x-x

I. Explain in brief:-

a) What is a data hazard? How to avoid it?

b) Computational granularity

c) CISC vs. RISC processor

d) Difference between data-parallel and object-oriented model

e) Busy-wait vs. Sleep-wait protocols (5x2)

UNIT – I

II. a) Consider a vector computer which can operate in one of the two execution modes at a time: one is the vector mode with an execution rate of R_v = 10 M flops, and the other is the scalar mode with an execution rate of R_s = 1 M flops. Let α be the percentage code that is vectorizable in a typical program mix for this computer.

i) Derive an expression for the average rate R_a for this computer.
ii) Plot R_a as a function of a in the range (0,1)
iii) Determine the vectorization ratio a needed in order to achieve an average execution rate of R_a = 7.5 M flops
iv) Suppose R_s =1 M flops and α = 0.7. What value of R_v is needed to achieve R_a= 2 Mflops?

b) How does a multiprocessor machine differ from multicomputer machine? Give two examples of each. (2x5)

III. a) Given the data below, what is the impact of second-level cache associativity on its miss penalty?

i) Hit time L2 for direct mapped = 10 clock cycles.
ii) Two-way set associativity increases hit time by 0.1 clock cycles to 10.1 clock cycles.
iii) Local miss rate L2 for direct mapped = 25%
iv) Local miss rate L2 for two-way set associative = 20%
v) Miss penalty L2 = 100 clock cycles.

P.T.O.

b) What are VL1W processors? Discuss the various problems associated with the VLIW processor and measures for their mitigation. (2x5)

IV. a) Explain and compare speedup performance-models.

b) What is cache coherence problem and when do you say a memory system is coherent? What are cache coherence protocols? (2x5)

UNIT – II

V. a) Answer the following questions on design choices of multicomputers made in the past;

i) Why are low-cost processors chosen over expensive processors as processing nodes?

ii) Why was distributed memory chosen over shared memory?

iii) Why was message passing chosen over address switching?

b) How do static and dynamic topologies of interconnection differ? Explain different factors affecting the performance of interconnection networks? (6+4)

VI. a) Explain the concurrent OOP and an actor model in object oriented model.

b) Draw and explain 16x16 Omega Network. Explain its routing technique with example. (2x5)

VII. a) Explain principles of various synchronous mechanisms for inter-process communications.

b) Write all Bernstein Conditions.

c) Draw and explain the Cray Y-MP or CM-2 architecture. (3+2+5)

x-x-x