Exam.Code:0906
Sub. Code: 6682

1108

B.E. (Electronics and Communication Engineering)
Second Semester
EC-203: Digital Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) What is the difference between SOP and POS?

b) Compare the various logic families according to propagation delay.

c) Counter outputs are always derived from Q and never from $\overline{Q}$. What might be the problem if we do so? Justify your answer.

d) What is the need for feedback in case of flip-flops and latches?

e) What will be the appropriate application areas of dual-slope ADCs? (5x2)

UNIT – I

II. a) Realize Y = A'B + B'C' + ABC using an 8-to-1 mux. Can it be realized with 4-mux?

b) Explain the working principle of a D-flip-flop in detail. (2x5)

III. a) Design a circuit which has 5 binary inputs (A,B,C,D,E), with A being the MSB. It must produce an output logic high for any prime number detected in the input data for its decimal equivalent.

b) Explain the complete design process involved in the designing of 3 bit binary to Gray code counter. (2x5)

IV. a) Design a mod-8 binary counter with parallel clock input using J-K flip-flops. Also explain your answer with the aid of waveforms.

b) Compare K-maps and Quine-MCCluskey methods in short. (8,2)

P.T.O.

UNIT – II

V. a) Three CMOS devices are cascaded, if each has a propagation delay time of 100 ns, what is the total propagation delay time?

b) Suppose you need a TTL device with a power dissipation of less than 5 mW per gate and a delay time of less than 20 ns. What TTL type would you choose?

c) Why are tri-state buffers necessary for some register? (3,4,3)

VI. a) Explain in detail the working principle of a parallel in parallel out register.

b) What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percent? (8,2)

VII. a) Write down a tabular comparison between the various characteristics of following digital logic families: TTL, ECL and CMOS.

b) Find the following for a 12-bit counter type ADC using 1 MHz clock.
i) Maximum conversion time
ii) Average conversion time (6,4)

x-x-x