Exam.Code:0906 Sub. Code: 6677

1108

B.E. (Computer Science and Engineering) **Second Semester** CS-203: Digital Electronics and Logic Design

Time allowed: 3 Hours

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Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

- I. Attempt the following:
 - a) Draw the logic circuit for the expression $F = \overline{A}B + A\overline{B}\overline{C}$.
 - b) Write the expression for Boolean function $F(A, B, C) = \sum m(1,4,5,6.7)$ in Standard product of sums (POS) form.
 - c) Minimize Y (A,B,C,D) = $\sum m(1, 3,5,7,9)$ using K-map...
 - d) Why TTL logic family is faster than DTL.
 - e) How demultiplexer can be used as decoder?
 - f) Draw the logic circuit of 3 to 8 line decoder.
 - g) Give the characteristic table of R.S and JK flip-flop.
 - h) What do you mean by FPGA device?
 - i) What is race around condition and how it can be eliminated?
 - j) Why asynchronous counters are called as ripple counters?

(10x1)

UNIT - I

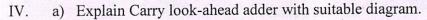
- f (A,B,C,D,E,F)II. variable function is given as $\pi M(6,9,13,18,19,25,27,29,41,45,57,61)$. Obtain the Minimal expression using Quine - McClusky minimization method.
 - Implement half subtractor using NAND gates.

(8,2)

- III. Explain open collector TTL gate.
 - b) Write a short note on CMOS NAND gate.

(5,5)

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b) Design a combinational circuit that will generate an even parity bit for 4 bit input and implement it using only NAND gates. (5,5)

UNIT - II

- V. a) Illustrate the working of Master-slave J-K flip-flop.
 - b) Implement the logic function $F(A,B,C,D) = \sum m(0,1,2,3,4,5,8,9,10,11,15)$ using 8x1 and 16x1 multiplexer. (5,5)
- VI. a) Design a synchronous 3-bit up-down counter using J-K. flip-flops.
 - b) Draw the logic diagram of a 4-bit parallel-in, serial-out shift register and explain its working. (5,5)
- VII. a) Design full adder and subtracter using PLA.
 - b) Write a short note on Johnson counter.

(6,4)