Exam.Code:0916
Sub. Code: 6785

1058

B.E. (Computer Science and Engineering)

Fourth Semester

CS-405: Computer Architecture and Organization

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Attempt the following:-

a) Gate delays in carry lookahead versus n-bit adder

b) Synchronous versus Asynchronous bus

c) Isolated I/O versus memory mapped I/O

d) RISC versus CISC architecture

e) Data hazard versus control hazards in pipelining **(5x2)**

UNIT – I

II. a) With a neat sketch explain the working principle of DMA.

b) Draw necessary diagrams and explain the control signal generation using micro programmed control. (2x5)

III. a) An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the virtual memory and in the main memory?

b) Explain with example how to multiply two unsigned binary numbers. (2x5)

IV. a) Explain a 4-stage instruction pipeline. Also explain the issues affecting the pipeline performance.

b) Describe the techniques for handling control hazards in pipelining. (2x5)

UNIT – II

V. a) What are the different secondary storage devices? Elaborate on any one of the devices.

b) What are handshaking signals? Explain the handshake control of data transfer during input and output operation. (2x5)

P.T.O.

VI. a) What is meant by bus arbitration? What is its role and why it is required? Explain with suitable, example.

b) How many memory chips are needed to construct 2 M x 16 memory system using 512 K x 8 static memory chips? Construct the architecture. (2x5)

VII. a) What is a mapping function? What are the ways the cache can be mapped?

b) Explain the Working of a Carry-Look Ahead adder. (2x5)

x-x-x