Exam.Code:0906
Sub. Code: 6682

1058

B.E. (Electronics and Communication Engineering)
Second Semester
EC-203: Digital Design

Time allowed: 3 Hours

Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Section.

x-x-x

1. a) state and explain duality theorem.

b) What is the difference between SOP and POS?

c) What are the major differences between TTL and CMOS devices?

d) What do you understand by racing condition and propagation delay.

e) What will be the appropriate application areas of dual-slope ADCs?

2 x 5 =10

SECTION-A

2. a) Suppose a truth table has a low output for the first three input conditions: 000, 001 and 010. If all other outputs are high, what is the product of sums (POS) circuit? 5

b) Design a circuit which has 5 binary inputs (A,B,C,D,E), with A being the MSB. It must produce an output logic high for any prime number detected in the input data for its decimal equivalent. 5

3. a) Draw the logic diagram, truth table and waveforms for a two flip-flop ripple counter operating in count-down mode. 8

b) What is the primary difference between a J-K and an R-S flip-flop. 2

4. a) Generate a simplified expression using Quine-McCluskey method for the following expression

$$Y = \sum m(2,5,6,7,8,9,14) + d(4,15)$$ 8

b) What is need for feedback in case of flip-flops? 2

SECTION-B

5. a) What is the resolution of a 9-bit D/A converter which uses a ladder network? What is the resolution expressed as a percent? If full-scale output voltage of this converter is +5 V, what is the resolution in volts? 3

b) Explain with the aid of block diagram the working principle of an ADC-counter method. 7

P.T.O.

6 a) Find the following for a 12-bit counter type ADC using 1 MHz clock.

(i) Maximum conversion time

(ii) Average conversion time

(iii) Maximum conversion rate 6

b) What are the major drawbacks of TTL technology. How CMOS is able to resolve it? And why MOS technology designated as unipolar, while TTL is designated as bipolar. 4

7. a) Define following TTL parameters

(i) Floating inputs (ii) worst case input voltages

(ii) worst case output voltages (iv) noise immunity 8

b) What are the various applications of serial in parallel out and parallel in serial out register. 2

x-x-x