**Exam.Code:0929**
**Sub. Code: 6357**

**1078**

**B.E. (Electronics and Communication Engineering)**
**Fifth Semester**
**EC-506: Integrated Circuits**

Time allowed: 3 Hours Max. Marks: 50

***NOTE:*** *Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Unit.*

*x-x-x*

I. Attempt the following:-

a) What are the various resistor and capacitor design guidelines for thin films?

b) Define miller indices? Draw 111 plane,

c) What is Solid Solubility?

d) What is LOGOS?

e) What is silicide?

f) Draw the doping profile obtained after ion implantation.

g) Define Sheet resistance.

h) What is self-defined structure in MOS?

i) What is Lift OFF process?

j) What is Latch-up in MOS? (10x1)

**UNIT – I**

II. a) Using plots discuss the general international technology trends for VLSI devices?
b) Describe the Czochralski crystallization process for producing single crystal silicon suitable for microelectronic production. What are the parameters a fabrication engineer is interested in while doing crystal growth.
c) With diagrams, discuss various roles of Si02 in IC, How Sio2 grown by thermal oxidation is different from CVD oxide? (3,3,4)

III. a) Discuss the process for fabricating Mask for Photolithography. What is step and repeat process?
b) Discuss reactive ion etching and its applications. Also compare wet and dry etching
c) Discuss the growth of Epitaxial, Si02 and Si3M4 layers using CvD process. (3,3,4)

P.T.O.

IV. Write a note on any two of the following:-

a) Diffusion and its various doping profile-

b) Fine Line Lithography techniques

c) Metallization and packaging (5x2)

## UNIT – II

V. a) Tell using diagrams, how the use epitaxial layer improves the working of devices

b) What is LOCOS? How it is used to provide isolation in BJT and MOS IC's?

c) Discuss isoplaner npn transistor structure. (3,4,3)

VI. a) Define threshold voltage of NMOS transistor? How it can controlled?

b) Discuss various ways of controlling Latch-up in MOS IC's.

c) With diagrams, discuss the fabrication of n-well CMOS with shielded source, drain and gate. What is the function of the field oxide and silicided regions. (3,3,4)

VII. Write a note on any two of the following:-

a) Twin-well CMOS fabrication process.

b) IC cross-overs and clean room standards.

c) Monolithic Capacitors. (2x5)

*x-x-x*