Exam.Code:0929
Sub. Code: 6909

1078

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-501/512: VLSI Design

Time allowed: 3 Hours Max. Marks: 50

NOTE: Attempt five questions in all, including Question No. 1 which is compulsory and selecting two questions from each Part.

x-x-x

Q1)	a) What are advantages of ICs over Discrete components? b) Compare isoptropic and anisotropic etching process. c) What are advantages of SiO_2? d) What are short channel effects? e) What is body bias effect in MOSFET? f) Define critical voltages in CMOS inverter VTC curve? g) Compare nMOS and CMOS Pass Transistor gate. h) Draw well-labeled Energy Band Diagram of MOS capacitor in depletion region. i) What is a symmetrical CMOS inverter? j) Design 4X1 multiplexer using Pass Transistor Logic.	10
	Part A	
Q2)	a) Why Silicon is the most commonly used material in semiconductor industry? b) What are various types of Diffusion? Define and discuss Fick's law of diffusion.	5 5
Q3)	a) What are various Isolation Techniques in ICs? b) Using labeled diagram, discuss the photolithography process steps? Compare the Positive and Negative photoresist.	5 5
Q4)	a) Discuss the nMOS fabrication process steps. What is self-aligned gate technology? b) What is stick diagram? ImplementY=((A+B)C)' using CMOS logic and draw its stick diagram.	5 5
	Part B	
Q5)	a) Derive the square law Id-Vds characteristics of nMOSFET. What is Channel length Modulation effect? b) What is voltage scaling and full-scaling in MOSFET?	6 4
Q6)	a) Calculate the propagation delay of CMOS inverter for Vdd=5V, V_{Tn}=0.4V, V_{Tp}=-0.4V, $\mu_n C_{ox}$=50μA/V²and $\mu_p C_{ox}$=20μA/V². $(W/L)_n$=20and $(W/L)_p$=50. Find if the inverter is symmetric or not. b) Discuss various region of operation of transistors in VTC curve of a Resistive load inverter. Compare it with CMOS inverter.	5 5
Q7)	a) What are the sources of Power dissipation in CMOS inverter? How these can be minimized? b) Compare the Transmission gate, CMOS logic and Clocked CMOS logic.	5 5

x-x-x