Exam.Code:0929
Sub. Code: 6913

1128

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-505: Digital System Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Explain the following:-

a) Digital Constraints

b) De-Morgan's theorem

c) Functions

d) Input variables

e) Name any two error detection technique

f) ASCII

g) Next state decoder

h) Types of FSMs

i) Cycles

j) State diagram (10x1)

UNIT – I

II. With the help of example, explain both tabular and iterative consensus method for obtaining implicants for single and multi-output functions. (10)

III. Explain different methods of detecting and locating faults in combinational circuit. (10)

IV. Explain error detection and error correction techniques. (10)

UNIT – II

V. Explain the concept of state diagram. With the help of example, explain machine minimization of FSMs. (10)

VI. Design a asynchronous circuit and also explain cycles and races with respect to that circuit. (10)

P.T.O.

VII. a) i) Convert the RS Flip Flop to a (a) D-LATCH

ii) T, and

iii) a D-LATCH to a T Flip-Flop.

b) Explain fault detection in sequential circuits. (5,5)

x-x-x