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Exam. Code: 0929
Sub. Code: 6909

1128

B.E. (Electronics and Communication Engineering)
Fifth Semester
EC-501: VLSI Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Part.

x-x-x

Q1) a) What are the sources of leakage power dissipation in MOSFET? 10
b) What are the factors that make Si the most attractive material in electronic device applications?
c) What are applications of Oxidation process?
d) How are Resistors fabricated in monolithic IC?
e) Briefly discuss the basic structure of a MOS transistor?
f) Define noise margin?
g) What are lambda based designed rules?
h) What are various short channel effects in MOSFET?
i) What is a symmetrical CMOS inverter?
j) Why Domino logic is called high performance logic?

Part A

Q2) a) Discuss crystal refining process in detail. What are various crystal defects? 5
b) Discuss the Ion implantation process. Compare it with diffusion process. 5

Q3) a) An enhancement type NMOS has the following parameters: V_{To} =0.8V, λ=0.05V^{-1}, k'=20$\mu A/V^2$. The current I_D=0.24mA when transistor is biased with V_G=2.8V, V_D=5V, V_S=1V and V_B=0V. Determine its W/L. 5
b) Derive expression of maximum depletion depth in nMOS. What are various parameters on which the threshold voltage depends? 5

Q4) a) Discuss the CMOS fabrication process steps. What is LOCOS? 5
b) Discuss the fabrication steps and diffusion profile of buried collector type BJT. What are its advantages over diffused BJT? 5

Part B

Q5) a) Compare the nMOS and CMOS PTL in detail? 5
b) Derive and analyze the expression for propagation delay (high to low) in CMOS inverter. 5

Q6) a) Derive expression for dynamic power dissipation in CMOS. How can the power dissipation be reduced? 5
b) Derive the expression of logical threshold and V_{IH} in CMOS inverter. Compare various inverter configurations. 5

Q7) a) Discuss the implementation of XOR using PTL. Compare it in terms of number of transistors in the conventional CMOS implementation. 5
b) Compare the Clocked CMOS and Conventional CMOS logic families. 5

x-x-x