3rd.18

Exam.Code:0921
Sub. Code: 6835

1128
B.E. (Information Technology)
Third Semester
ITE-374/343: Digital Electronics

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: *Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.*

x-x-x

I. Answer the following:-

a) Give the excitation table ofJK flip flop.

b) Simplify: Y(A,B,C) = ABC + AB' + ABC'

c) What is the need for hamming code?

d) Define Noise Margin. Is it good to have low noise margin?

e) What is the need for Sample and Hold switch? (5x2)

UNIT – I

II. Implement Full adder using 4:1 multiplexer. (10)

III. Design a sequence generator to generate the sequence 0 → 2 → 5 → 4 →7→ 0 using JK flip flops. Avoid lockout condition such that each unused state falls to its immediate next state. (10)

IV. a)Find 723_8 + 6AFH

b) Write the gray codes for decimal digits 0-9.

c) Minimize using K-Map Y(A,B,C,D) = ΠM(l,2,3,5,6,7,9,10,l 1,13,14,15)

UNIT – II

V. a) Find the output voltage of a 4 bit R-2R ladder type DAC, having digital input of 1010 and maximum voltage of 10V.

b) Describe the specifications of a DAC that are important in the choice of the same. (5,5)

P.T.O.

VI. Design NOR and NAND gates using CMOS. What is the advantage offered by CMOS over MOS? (10)

VII. a) Explain the salient features of SRAM.

b) Find all the equivalent states using Implication Table

	XY = 00	01	11	10	
a	a	c	e	d	0
B	d	e	e	a	0
C	e	a	f	b	1
D	b	c	c	b	0
E	c	d	f	a	1
f	f	b	a	d	1

(5,5)

x-x-x