Exam.Code:969
Sub. Code: 7339

1128

M.E. (Electronics and Communication Engineering)
First Semester
ECE-1104: Digital System Design

Time allowed: 3 Hours **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Attempt the following:-

a) Define the term mask programming.

b) Mention any two problems in asynchronous sequential circuits.

c) What are the advantages of FPGAs?

d) How is an MDS diagram different from a state diagram?

e) What are stuck- at faults? (5x2)

UNIT – I

II. a) Describe the various specifications of a D/A converter.

b) What are the different errors that come up during Analog to Digital conversion? (2x5)

III. a) Implement the logic function F(A, B, C, D) = Σ(0,1, 3,4, 8,9,15) using a 4:1 MUX.

b) How does the architecture of PLA differ from ROM and PAL? (2x5)

IV. a) Write a VHDL program for a full adder using behavioral modelling.

b) What are the various blocks of an ALU? How can it be implemented on an FPGA? Explain briefly. (2x5)

UNIT – II

V. a) Design a sequence detector that produces an output 1 whenever the sequence 101101 is detected.

b) What are the phases of design while designing system controller? How is the controller architecture chosen? (2x5)

P.T.O.

VI. Design an asynchronous circuit that will output only the second pulse received whenever a control input is asserted from LOW to HIGH state. Any further pulses will be ignored. (10)

VII. Explain the concepts of controllability and observability in design for testability. Explain any test technique used at the system level. (10)

x-x-x