Exam.Code:0999
Sub. Code: 7622

1128
M.E. (Computer Science and Engineering)
First Semester
Elective – II
CS-8109: Advanced Computer Architecture

Time allowed: 3 Hours   **Max. Marks: 50**

NOTE: Attempt five questions in all, including Question No. I which is compulsory and selecting two questions from each Unit.

x-x-x

I. Distinguish between the following:-

  a) Arithmetic and instruction pipeline

  b) Ring vs. Chordal ring

  c) Blocking vs. Non-blocking networks

  d) Hardwired vs. microcode control

  e) Scalar and vector pipeline   (5x2)

UNIT – I

II. a) What is pipelining? List pipeline hazards. Explain one in detail.

  b) Briefly discuss the three design issues of parallel structure.

  c) Define cache coherence problem. Suggest and explain a method to eradicate it.
                                                            (3,2,5)

III. a) What are semaphores and their applications in parallel computing? Compare Binary and Counting semaphores.

  b) State Amdahl's law. Compare it with other two laws of performance metrics for parallel computers.   (4,6)

IV. a) Explain the architectural operations in SIMD and MIMD computers. Distinguish between multiprocessor and multicomputers based on their structures.

  b) Assume we have a computer where CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the miss penalty is 25 cycles and miss rate is 2% how much faster would be computer if all instructions were cache hits?   (5,5)

P.T.O.

UNIT – II

V. a) Draw and explain the Cypress CY7C602 floating point unit. Compare it will CY7C601 SPARC processor. (7)

   b) Explain the Snoopy Bus Protocol with labeled diagrams. (3)

VI. a) Explain the following terms associated with cache design:
   i) Write-through vs. write-back caches
   ii) Factors affecting cache hit ratios

   b) Given an unpipelined processor with a 10ns cycle time and pipeline latches with 0.5ns latency, what are the cycle times of pipelined versions of the processor with 2,4,8 and 16 stages if the datapath logic is evenly divided among the pipeline stages? Also, what is the latency of each of the pipelined versions of the processor? (5,5)

VII. a) What are vector-access memory schemes? Compare the three-memory organization.

   b) Draw and explain the CM-2 architecture. Explain in detail that how the nodes are processed in CM-2? (5,5)

x-x-x